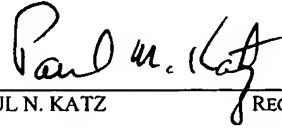


PATENT

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APPLICATION FOR LETTERS PATENT

FOR

HIGH VOLTAGE ESD-PROTECTION STRUCTURE

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HIGH VOLTAGE ESD-PROTECTION STRUCTURE

Field of the Invention

[0001] The present invention relates generally to semiconductor integrated circuits, and more particularly to protection of the semiconductor integrated circuits from electrostatic discharge (ESD).

Background of the Invention Technology

[0002] Modern electronic equipment uses digital semiconductor integrated circuits for operation thereof. The digital semiconductor integrated circuits receive inputs from various sources, *e.g.*, pushbuttons, sensors, *etc.*, and have outputs that control operation of the equipment based upon the various inputs thereto. The inputs and outputs of the semiconductor integrated circuits may be subject to undesirable high voltage electrostatic discharge (ESD) in addition to the desired input or output signal level. The ESD, characterized by fast transient high voltage discharges, may be from static electricity generated by a user of the equipment, equipment handling, power supply voltage transients and the like. An ESD event may create a sufficiently high voltage to cause destructive breakdown of transistor devices connected to the inputs and/or outputs of the semiconductor integrated circuits.

[0003] Semiconductor integrated circuits are becoming functionally more capable and are operating at faster speeds. The increased functional capability is the result of higher transistor count in each integrated circuit, thereby allowing the operation of more sophisticated software and/or firmware to produce the many features available in the equipment. The faster operating speeds further enhance the operation of the equipment. In order to keep integrated circuit die size within a reasonable cost, the electronic circuits therein must be more densely

concentrated in as small an area as possible, thus the many transistors making up the electronic circuits within the integrated circuit must be made as small as possible. As these transistors become smaller and smaller, the spacing of the parts of each transistor, *e.g.*, source, gate, drain, becomes smaller, as does the dielectric thickness of the insulation between these parts. The extremely thin dielectric is very susceptible to damage by excessive voltages present in an ESD event that may cause destructive breakdown of an input and/or output device. Also, as operational speeds increase, the need for low capacitance structures becomes more important.

[0004] Various voltage protection circuits have been used to limit the peak voltage at an input and/or output of an integrated circuit. Attempts have been made to incorporate ESD protection within the integrated circuit, but are either not very effective, and/or require a significant amount of area within the integrated circuit die. When an ESD event occurs, some ESD protection circuits will remain conductive to ground at a lower voltage than what initially triggered conduction in the ESD protection circuit. This is called "snapback" and is undesirable, especially when an input and/or output is adapted for high voltage operation (voltage being higher than a normal logic voltage level). Use of the breakdown voltage of a diode for ESD protection has no snapback problems but lacked sufficient current handling for most ESD events.

[0005] Therefore, what is needed is an ESD protection circuit integral within the integrated circuit die that is effective in protecting sensitive input and/or output circuits from an ESD event that may cause destructive breakdown, has enough current handling capabilities during the ESD event and does not snapback from the ESD event occurrence.

SUMMARY OF THE INVENTION

[0006] The invention overcomes the above-identified problems as well as other shortcomings and deficiencies of existing technologies by providing a high voltage ESD-protection structure that is effective in protecting sensitive input and/or output circuits from an ESD event by having a controlled breakdown at a voltage that is less than a voltage that may cause destructive breakdown of the input and/or output circuits, has enough current handling capabilities during the ESD event and does not snapback from the ESD event occurrence.

[0007] According to an embodiment of the invention, a high voltage ESD-protection structure may advantageously be located substantially under an integrated circuit bond pad. The high voltage ESD-protection structure protects the delicate transistor circuits connected to the bond pad from destructive high voltage ESD events by having a controlled breakdown at a voltage that is less than a voltage that may cause destructive breakdown of the input and/or output circuits. The high voltage ESD-protection structure is able to absorb high current from these ESD events without snapback that would compromise operation of the higher voltage inputs and/or outputs of the integrated circuit. The ESD-protection structure will conduct whenever an ESD event occurs at a voltage above a controlled breakdown voltage of an electronic device, *e.g.*, diode, in the ESD-protection structure. Conduction of current from an ESD event having a voltage above the electronic device controlled breakdown voltage may be through another electronic device, *e.g.*, transistor, having high current conduction capabilities, in the ESD-protection structure that may be controlled (triggered) by the device (*e.g.*, diode) determining the controlled breakdown voltage (at which the ESD voltage is clamped to a desired value).

[0008] According to embodiments of the invention, a PNP transistor may be connected to an input and/or output pad of an integrated circuit device. The base of the PNP transistor may be connected to a diode having a controlled breakdown voltage having a desired trigger controlled breakdown voltage. When a voltage from an ESD event occurs that is greater than the controlled breakdown voltage of the electronic device, *e.g.*, diode, the controlled breakdown voltage will cause the PNP transistor to conduct, *e.g.*, from the input and/or output pad to ground. Since the PNP transistor structure is capable of conducting high transient currents, the PNP transistor structure will effectively and safely shunt any destructive voltage ESD event to ground. When the voltage at the ESD event voltage is below the controlled breakdown voltage, the PNP transistor will turn off and will not remain in a snapback condition, thus returning the input and/or output pad to full normal voltage operation.

[0009] According to embodiments of the invention, an ESD-protection structure may, but is not limited to, be located substantially under an integrated circuit bond pad in which further a low capacitance structure is formed by creating a forward diode between the bond pad and the ESD clamp circuit. Placing an ESD-protection structure under the bond pad may eliminate parasitic substrate capacitance. Furthermore a parasitic PNP transistor may be formed from the inserted forward biased diode.

[0010] An embodiment of the invention comprises a semiconductor structure of a plurality of first P+ diffusions, each of the plurality of first P+ diffusions is surrounded by a first N+ diffusion. The plurality of first P+ diffusions and the first N+ diffusion are located substantially under a bond pad to be ESD protected. The P+ diffusions may be shaped in squares, rectangles, stripes and the like (other shapes and are also contemplated herein), and may

be connected to the conductive bond pad with conductive vias through an insulating layer located between the bond pad, the plurality of first P+ diffusions and the N+ diffusion. The first N+ diffusion surrounds each of the plurality of first P+ diffusions. The first N+ diffusion is insulated from the bond pad by the insulating layer. A first N- well is located in a P- well of the integrated circuit and substantially under the first N+ diffusion and the plurality of first P+ diffusions. The P- well may be a P- substrate of an integrated circuit, or the P- well may be a P- well in an N- substrate of an integrated circuit.

[0011] A second N- well is located in the P- well and adjacent to the first N- well. A second N+ diffusion and a second P+ diffusion are located in the second N- well. The second N+ diffusion is connected to the first N+ diffusion with a conductor. A third P+ diffusion encircles the first and second N+ and P+ diffusions and is located in the P- well. The third P+ diffusion and second P+ diffusion are connected together with a conductor. The second and third P+ diffusions may be connected to ground by a conductive connection, *e.g.*, metal or low resistance semiconductor material. It is contemplated and within the scope of the invention that more than one second N+ diffusion, and more than one second and third P+ diffusion may be utilized in the ESD-protection structure

[0012] Capacitance of the above described ESD-protection structure embodiment is minimal because the only capacitance seen by the bond pad is the P+ diffusions to N- well and the N+ and P+ diffusions/N+ diode junction capacitance. The bond pad to the P- well capacitance is substantially reduced by the ESD-protection structure being mostly under the bond pad. Other ESD structures not necessarily having reduced capacitance may also be equally effective so long as the current carrying capacity and non-snap back attributes are maintained.

One of ordinary skill in the art and having the benefit of this invention disclosure can implement many other ESD protection structures have a substantially fixed breakdown voltage value and a high current capacity shunt connected to a node to be ESD protected.

[0013] The invention ESD-protection structure clamps a voltage transient with a non-snapback trigger. The bond pad voltage to ground increases until the N+ diffusion to P- well diode breaks down (conducts). The bond pad voltage will therefore be a diode drop above this breakdown voltage. The ESD-protection clamping operation is enhanced by the vertical PNP parasitic structure formed from the P+ diffusions, the N- well and the P- well. The ESD transient current flows directly to the P- well due to the presence of the aforementioned vertical PNP parasitic structure.

[0014] A technical advantage is high current clamping of ESD transients. Another technical advantage is enhanced high voltage ESD clamping by the vertical PNP parasitic structure. Still another advantage is protection of higher voltage input and outputs of an integrate circuit. Yet another advantage is a non-snapback triggering of the ESD-protection clamping. Another technical advantage is reduce size for an ESD structure. Yet another technical advantage is isolating the bond pad from the substrate capacitance. Another technical advantage is reduced capacitance at a input or output node.

[0015] Features and advantages of the invention will be apparent from the following description of the embodiments, given for the purpose of disclosure and taken in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

[0016] A more complete understanding of the present disclosure and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawing, wherein:

[0017] Figure 1a illustrates a schematic diagram of a sectional elevational view of a high voltage ESD-protection structure, according to an exemplary embodiment of the invention;

[0018] Figure 1b illustrates a schematic diagram of a plan view of the high voltage ESD-protection structure shown in Figure 1a;

[0019] Figure 1c illustrates a schematic diagram of a plan view of another exemplary embodiment of the high voltage ESD-protection structure shown in Figure 1a; and

[0020] Figure 2 illustrates a schematic circuit diagram of the high voltage ESD-protection structure of Figure 1.

[0021] While the present invention is susceptible to various modifications and alternative forms, specific exemplary embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0022] Referring now to the drawings, the details of exemplary embodiments of the present invention are schematically illustrated. Like elements in the drawing will be represented by like numbers, and similar elements will be represented by like numbers with a different lower case letter suffix. P- refers to lighter doped p-silicon, P+ refers to heavier doped p-silicon, N- refers to lighter doped n-silicon, and N+ refers to heavier doped n-silicon, wherein p-silicon has a plurality of positive immobile silicon ions, and n-silicon has a plurality of negative immobile silicon ions.

[0023] Referring to Figure 1, depicted is a schematic diagram of a high voltage ESD-protection structure, according to an exemplary embodiment of the invention. Figure 1a illustrates a sectional elevational view, Figure 1b illustrates a plan view of the high voltage ESD-protection structure, and Figure 1c illustrates a plan view of another high voltage ESD-protection structure. A semiconductor integrated circuit comprises many transistors, inputs and outputs. The high voltage ESD-protection structure shown in Figure 1 may be advantageously used for both inputs and outputs of the integrated circuit to protect the delicate transistors connected thereto.

[0024] The high voltage ESD-protection structure of Figure 1, generally represented by the numeral 100, comprises a plurality of first P+ diffusions 126 surrounded by a first N+ diffusion 128. The plurality of first P+ diffusions and the first N+ diffusion are located substantially under a bond pad 114 to be ESD protected. The plurality of first P+ diffusions 126, may be rectangular or square (see Figure 1b) or may be arranged in stripes (see Figure 1c), and are connected to the bond pad 114 with conductive vias 116 through an insulating layer 124 located between the bond pad 114, the plurality of first P+ diffusions 126 and the first N+

diffusion 128. Other shapes for the plurality of first P+ diffusions 126 may be used and are contemplated herein. The first N+ diffusion 128 is insulated from the bond pad 114 by the insulating layer 124. A first N- well 130 is located substantially under the first N+ diffusion 128 and the plurality of first P+ diffusions 126. The integrated circuit substrate 132 may comprise P- semiconductor material that behaves as a P- well. The integrated circuit well 132 comprises P- semiconductor material of which the first N- well 130 is located therein. In addition, the N+ diffusions 128 may be connected together by conductive vias connected together by conductive paths (not shown).

[0025] A second N- well 140 is located in the P- well 132 and adjacent to the first N- well 130. A second N+ diffusion 138 and a second P+ diffusion 136 are located in the second N- well 140. The second N+ diffusion 138 is connected to the first N+ diffusion 128 with conductor 122 and vias 116. A third P+ diffusion 134 encircles the first and second N+ and P+ diffusions and is located in the P- well 132. The third P+ diffusion 134 and second P+ diffusion 136 are connected together with conductor 120 and vias 116. The second P+ diffusion 136 and third P+ diffusion 134 may be connected to ground with a conductive connection, *e.g.*, metal or low resistance semiconductor material.

[0026] A PNP transistor 102 may be formed with the first P+ diffusions 126 being the emitter, the first N- well 130 being the base and the P- well 132 being the collector. A diode 104 may be formed with the second P+ diffusion 136 (anode) and the second N+ diffusion 138 (cathode). The cathode of diode 104 may be coupled to the first N- well 130 (base of transistor 102) through conductive vias 116 and conductor 122. Generally, the P- well 132 is coupled to

ground (and/or a negative rail of a power source) and functions like a resistance to ground, generally represented by resistor 110.

[0027] Capacitance of the above described high voltage ESD-protection structure 100 is minimal because the only capacitance seen by the bond pad 114 is the first P+ diffusions 126 to first N- well 130 which forms a diode junction capacitance. The bond pad metal 114 to the P- well 132 capacitance is substantially reduced because the high voltage ESD-protection structure 100 is substantially under the bond pad 114.

[0028] Referring to Figure 2, depicted is a schematic circuit diagram of the high voltage ESD-protection structure of Figure 1. The invention high voltage ESD-protection structure 100 clamps a high voltage transient on the bond pad 114 without snapback. For a positive high voltage transient, the PNP transistor 102 will conduct to ground when the controlled breakdown voltage of the diode 104 is exceeded. The positive high voltage transient will be clamped to a diode junction voltage (*e.g.*, about 0.7 volts) above the controlled breakdown voltage of diode 104. Since the area of the PNP transistor 102 is comprised of the plurality of first P+ diffusions 126 (emitter), the first N- well 130 (base) and the P- well 132 (collector), fairly substantial currents may be handled by the invention high voltage ESD-protection structure 100.

[0029] The invention, therefore, is well adapted to carry out the objects and attain the ends and advantages mentioned, as well as others inherent therein. While the invention has been depicted, described, and is defined by reference to exemplary embodiments of the invention, such a reference does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is capable of considerable modification, alternation, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent arts and having the

benefit of this disclosure. The depicted and described embodiments of the invention are exemplary only, and are not exhaustive of the scope of the invention. Consequently, the invention is intended to be limited only by the spirit and scope of the appended claims, giving full cognizance to equivalents in all respects.